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[illegible]6) Publications cited in the examination process  
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GB 22 86 950 A  
= WO 36 36 104 A1  
EP 02 70 160 A1  
= DE 3 7 88 85 8T2

54) Transceiver

57) A transceiver with a first mixer (M1) for the output signal of an input amplifier (LNA) and the output of a first fixed frequency local oscillator (LO1), with the resulting first intermediate frequency (ZF1) being fed to the mixing stages (M2I, M2Q) of a double down mixer in the base band (BB) with an adjustable local oscillator (LO2), having a double up mixer (M3I-M3Q), after the low pass filters (TPI, TPQ), whose two mixing stages (M3I, M3Q) are fed the I or Q signal, respectively, as well as signals of a third fixed frequency local oscillator (LO3), to form a second intermediate frequency (ZF2), a summer (SUM) for addition of the I and Q signals of the second intermediate frequency to a signal with a constant envelope, and having a subsequent limiting stage (LIM), which is followed by a demodulator (DEM) as an evaluation circuit, with, in transmit mode, the signals to be transmitted fed to the adjustable local oscillator (LO2) for their modulation, a transmitting mixer (MS) being provided, to which the modulated output signal of the adjustable local oscillator (LO2) as well as the output signal of first fixed frequency oscillator (LO1) are fed, and the output signal of the transmitting mixer (MS) being available as the transmitting signal after amplification in a transmitting amplifier (SV).

[see source for figure]

## Description

The invention concerns a receiver circuit, for the reception of high-frequency radio signals, having an input filter and, following this, a low-noise input amplifier with a double mixer, to which the HF signal and the output of a local oscillator are fed, for generation of I and Q components, with low pass filters for the I and Q components and with an evaluation circuit for the I and Q signals.

Furthermore, the invention concerns a transceiver which uses this type of receiver circuit.

Receiver/transmitter concepts for the reception of FSK-modulated high-frequency signals, particularly in frequency ranges of a magnitude of GHz, such as those which are suitable for mobile telephones and pagers, cannot be completely integrated on a semiconductor chip, because, for realization of the required selectivity, appropriate filters, such as surface acoustic wave (SAW) filters, are required, which, as such, stand in the way of complete integration. Other problems which confronts integration in an IC component are the requirements in regard to low phase jitter for the oscillators.

A possible solution is to implement the receiver as a homodyne receiver, in order to avoid IF filters, which—compared with the other components of a receiver—are relatively large and expensive. However, problems regularly arise hereby in the realization of the required automatic gain control (AGC).

A suggested solution for a homodyne receiver can be inferred from GB 2 286 950 A (Roke Manor). In this case, the input signal, after filtering and amplification, is fed to a double mixer, i.e., two mixers which work with an output signal of a local oscillator and/or with the output signal rotated by 90°, so that an I and a Q signal are generated. The I and the Q signal are each carried via a low pass filter. The subsequent evaluation circuit uses adders and limiters in order to obtain a total of four output signals, which in turn represent eight phase states, each rotated by 45° relative to one another, and which are fed to a decoder circuit. In the document, a circuit is also described which leads to a total of 16 phase states, but the expense for limiters, for example, becomes ever larger. Typically, the previously described receiver circuit is primarily intended for low data rates, e.g., in pagers.

A similar receiver circuit, which provides special measures to prevent the PLL from locking on at incorrect frequencies, is described in EP 0 270 160 (Siemens Telecommunicazioni).

A task of the invention is to create a receiver and/or transmitter circuit which allows a very high degree of integration in transceivers without the problems with a gain control or phase jitter occurring.

This object is achieved with a receiver circuit of the type initially described which, according to the invention, is characterized by a first mixer for the formation of a first intermediate frequency, to which the output signal of the input amplifier and the output of a first fixed frequency local oscillator is fed, with the first intermediate frequency being fed to the two mixing stages of the double mixer, whose local oscillator is adjustable and which is implemented as a down mixer in the base band, a double up mixer following the low pass filters,

whose two mixing stages are fed the I or Q signal, respectively, as well as the output or the output phase rotated by  $90^\circ$  of a third fixed frequency local oscillator, respectively, for formation of a second intermediate frequency, a summer for addition of the upwardly mixed I and Q signals of the second intermediate frequency into a signal with a constant envelope, and a limiting stage for the composite signal of the second intermediate frequency, which is followed by a demodulator as an evaluation circuit.

The invention offers the advantage that it leads to a tunable receiver in which, however, due to the fixed first oscillator frequency, a low phase jitter can be realized and, due to the combination of the I and Q components into a signal with a constant envelope, the question of automatic gain control also moves into the background.

In a suitable embodiment of the invention, an FSK modulator is present and the demodulator is implemented as a frequency discriminator.

Furthermore, an improvement of the reception performance results if a notch filter is provided before the first up mixer for suppression of interference and noise signals on the image frequency.

For this purpose, it is also recommended that an amplifier stage for this first intermediate frequency be provided between the first up mixer and the first double mixer.

For the purpose of extensive integration on one chip, a transceiver with a receiver according to the invention is advantageous in which, in transmit mode, the signals to be transmitted are fed to the adjustable local oscillator for their modulation, a transmitting mixer is provided, to which the modulated output signal of the adjustable local oscillator and the output signal of the first fixed frequency oscillator are fed, and the output signal of the transmitting mixer is available as the transmitting signal after amplification in a transmitting amplifier.

The emission of undesired frequencies can hereby be avoided without additional expense if, in transmit mode, the transmitting signal is fed to the antenna via the input bandpass filter.

For band limiting of the signal data to be transmitted, it is advantageous if the signals to be transmitted are fed to the adjustable local oscillator via a filter. An FSK modulator is recommended, with this filter, particularly for a DECT system, able to be a gauss filter.

The invention, including further advantages, will be described in the following with reference to an exemplary embodiment, which is illustrated in the drawing. In the drawing, the single figure shows a simplified block diagram of a transceiver according to the invention.

From the block diagram, one can see that a high-frequency signal, e.g., in the range of 1.8 GHz, arriving from an antenna ANT reaches a first transmitting/receiving transfer switch S1 via a bandpass filter BP and, if the switch S1 is set to the receive setting, as shown, the input of a low-noise input amplifier LNA. From here, the signal is fed to a notch filter NF1 in order to suppress interference signals and noises on the image frequency.

This is followed by a first mixing stage with a mixer M1, in which the amplified and filtered input signal is mixed with a first frequency  $f_{01}$  of a first local oscillator LO1 at a first intermediate frequency ZF1, e.g., in the range of 110 MHz. This first local oscillator LO1 is operated at a fixed frequency, which—corresponding to the first intermediate frequency—also lies in the GHz range.

It is hereby possible, in spite of the high frequency, to create an integratable synthesizer/oscillator with a PLL, in which a VCO (not shown) is coupled over a wide frequency range to a reference oscillator (not shown). Because the phase jitter of a synthesizer within its loop bandwidth is determined by the phase jitter of the reference oscillator, very good phase jitter can be realized within the frequency range of interest. This is independent of the process-conditioned limitations of IC technology, which also leads to the integratability mentioned.

In an intermediate frequency amplifier ZFV following the mixer M1, the first intermediate frequency signal is buffered and fed to a double mixer M2I-M2Q, namely a mixing stage M2I and a mixing stage M2Q. This double mixer is assigned a second local oscillator LO2, which is adjustable and serves for channel selection. The oscillator signal with the frequency  $f_{02}$  is fed directly to the mixing stage M2I for the purpose of forming an I component I and is fed to the mixing stage M2Q via a  $90^\circ$  phase shifter PH1 for the purpose of forming a Q component Q.

The double mixer M2I-M2Q mixes the first intermediate frequency down into the base band BB, in the range of 100 kHz, with its I and Q components then subjected to channel filtering in integrated low pass filters TPI and TPQ.

Because, as already mentioned initially, demodulation of complex signals present as I and Q components is costly, the I and Q components are, after filtering, mixed back up from the base band BB to a second intermediate frequency ZF2 in the range of, e.g., 10 MHz in a third mixer, a double mixer M3I-M3Q. For this purpose, two mixing stages M3I and M3Q are provided for the I and Q components, respectively, of the base band, as well as a third local oscillator, whose output signal, having a fixed frequency  $f_{03}$ , is fed to one mixing stage directly and to the other after  $90^\circ$  phase rotation in a phase shifter PH2.

The I and Q components thus arising through mixing are combined in a summer SUM into a "constant envelope" signal, i.e., a signal with a constant envelope, and this can now be limited in a known way in a limiter LIM. The limiter is followed by a demodulator DEM, specifically a frequency discriminator, at whose output the reception signal  $s_E$  is available. A field strength indication signal RSSI can, for example, be obtained in the limiter LIM, before signal limitation, of course.

The essential parts of the transmission path are shown in the block diagram below. A signal to be transmitted  $s_s$ , i.e., a data signal, is band limited in a filter FIL. In a DECT system, this filter is a gauss filter. The adjustable second local oscillator LO2 following the filter FIL is implemented in such a way that it can be directly FSK-modulated in transmit mode by the filter signal  $s_s$ . The modulated output signal reaches, via the switch S2, which, in transmit mode, is in the position indicated by the dashed line, a transmitting mixer MS, to which is fed, furthermore, the signal of a first fixed local oscillator LO1, whereby the modulated output signal is mixed up into the transmission band and, after amplification in a transmitting amplifier SV, is fed to the antenna ANT via the switch S1 and the bandpass filter BP.

It should be emphasized here that this is merely an exemplary embodiment that is being described, and only in a simplified form. Actually, those skilled in the art will, in the framework of their knowledge, insert necessary or appropriate amplifier stages, regulating circuits, filters, etc. in suitable places. The invention

is particularly advantageously usable in all receivers, particularly transceivers, which receive and/or transmit digital data using an FSK modulator, for example DECT systems, and in which an extensive integration of the components is desired.

#### Patent claims

1. Receiver circuit for the reception of high-frequency radio signals, having an input filter (BP) and a low-noise input amplifier (LNA) following this, having a double mixer (M2I-M2Q), to which the high-frequency signal and the output of a local oscillator (LO2) are fed, for generation of an I and a Q component, having first filters (TPI, TPQ) for the I and Q components, and having an evaluation circuit (LIM, DEM) for the I and Q signals,

#### **characterized by**

- a first mixer (M1), for the formation of a first intermediate frequency (ZF1), to which is fed the output signal of the input amplifier (LNA) as well as the output of a first fixed frequency local oscillator (LO1),
  - with the first intermediate frequency (ZF1) being fed to both mixing stages (M2I, M2Q) of the double mixer, whose local oscillator (LO2) is adjustable and which is implemented as the down mixer in the base band (BB),
  - a double up mixer (M3I-M3Q), following the first filter (TPI, TPQ), whose two mixing stages (M3I, M3Q) are fed the I or the Q signal, respectively, as well as the output or the 90° phase-shifted output, respectively, of a third fixed frequency local oscillator (LO3) to form a second intermediate frequency (ZF2),
  - a summer (SUM) for the addition of the upwardly mixed I and Q signals of the second intermediate frequency into a signal with a constant envelope, and
  - a limiting stage (LIM) for the combined signal of the second intermediate frequency, which is followed by a demodulator (DEM) as the evaluation circuit.
2. Receiver circuit according to claim 1, characterized in that an FSK modulator is present and the demodulator (DEM) is implemented as a frequency discriminator.
  3. Receiver circuit according to claim 1 or 2, characterized in that a notch filter (NFI) for suppression of interference and noise signals on the image frequency is provided before the first up mixer (M1).
  4. Receiver circuit according to one of the claims 1 to 3, characterized in that an amplifier stage (ZFV) for the first intermediate frequency (ZF1) is provided between the first up mixer (M1) and the first double mixer (M2).
  5. Transceiver with a receiver according to one of the claims 1 to 4, characterized in that in transmit mode the signals to be transmitted are fed to the adjustable local oscillator (LO2) for their modulation, a transmitting mixer (MS) is provided, to which the modulated output signal of the adjustable local oscillator (LO2), as well as the output signal of the first fixed frequency oscillator (LO1), are fed, and the output signal of the transmitting mixer (MS) is

- available as the transmitting signal after amplification in a transmitting amplifier (SV).
6. Transceiver according to claim 5, characterized in that, in transmit mode, the transmitting signal is fed to the antenna (ANT) via the input filter (BP).
  7. Transceiver according to claim 5 or 6, characterized in that the signals to be transmitted ( $s_s$ ) are fed to the adjustable local oscillator (LO2) via a second filter (FIL).
  8. Transceiver according to one of the claims 5 to 7, characterized by an FSK modulator.
  9. Transceiver according to claim 7 or 8, characterized in that the filter (FIL) is a gauss filter.
  10. Transceiver according to one of the claims 1 to 9, characterized in that the first filters (TPT [sic], TPQ) are low pass filters.
  11. Transceiver according to one of the claims 1 to 10, characterized in that the input filter (BP) is a bandpass filter.

1 page(s) of drawings attached

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DRAWINGS PAGE 1

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